[0081] Processing steps in the fabrication of semiconductor devices in accordance with some embodiments of the present invention will be discussed with respect to FIGS. **7**A through **7**E. Referring first to FIG. **7**A, the substrate **10**, buffer layer **20**, barrier layer **22** and spacer layer **23** are formed using similar processing steps as discussed above with respect to FIG. **1**A. Furthermore, the two-dimensional electron gas (2-DEG) **33** is formed at the heterojunction of two semiconductor materials (barrier layer **22** and buffer layer **20**) with different bandgap energies, and where the smaller bandgap material has a higher electron affinity as also discussed above with respect to FIG. **1**A. Accordingly, details with respect to the formation of these elements will not be discussed further herein.

[0082] Referring now to FIG. **7**B, the spacer layer **23** is patterned and etched using a mask **31**. The mask **31** may include a photoresist and/or a metal, and may be patterned using conventional photolithographic/liftoff techniques without departing from the scope of the present invention. In particular, the spacer layer **23** is etched to form a trench **76**. As illustrated, the trench extends through the spacer layer **23** and exposes a portion of the barrier layer **22**. In some embodiments of the present invention, the barrier layer **22** may be etched during formation of the trench **76**. In these embodiments, the trench **76** may extend from about 0 Å to about 200 Å into the barrier layer **22**.

[0083] Referring now to FIG. **7**C, with the mask **31** still in place, ions **500** are implanted into the surface of the barrier layer **22** exposed by the etch of the trench **76** to provide a gate implant region **510**. In some embodiments of the present invention, the implant energy may be chosen so that the resulting distribution of implanted elements may be predominantly located in the barrier layer **22**, and limiting the concentration of implanted elements that extend into the buffer layer **20** to very low levels. Thus, the structural damage associated with the ion implantation may be reduced near the interface between the barrier layer **22** and the buffer **20**, near the 2-DEG **33**. Accordingly, high mobility may be may be provided in the 2-DEG **33**.

[0084] In particular, the implanted element (ions) may be chosen such that it results in negative space charge once implanted into the barrier layer **22**. One possible implant element may include Magnesium (Mg). Mg, if situated on a group III lattice site in an AlGaN layer, serves as an acceptor, which may result in negative space charge when depleted. Other suitable implant elements may include, for example, Fluorine (F) or zinc (Zn). The implant energy may be from about 3.0 keV to about 10 kEV. The implant dose may be chosen such that the band bending shifts the threshold voltage to a positive value. Suitable implant doses may be, for example, from about from about 5.0×10^{12} cm^{-2} to about 1.0×10^{14} cm^{-2}. There is a limit to how far positive the threshold voltage can be shifted. When a certain implant dose is exceeded, the resulting band bending can cause the valence band in the barrier layer **22** to cross the Fermi-level at zero gate bias. This may lead to hole formation, which may cause device dispersion and/or threshold voltage drift during device operation.

[0085] After the ions **500** are implanted to form the implanted gate region **510**, the implanted gate region **510** may be annealed to recover lattice damage caused by the implant. The anneal may also serve to move the implanted elements into electrically active lattice sites, for example, from an interstitial site to a Group-III site in an AlGaN layer. The implant anneal may be performed at a temperature of from about 1000° C. to about 1300° C., which is near or above the typical MOCVD growth temperature for AlGaN and GaN. The implant anneal may be performed for from about 30 seconds to about 10 minutes. In some embodiments of the present invention, the implant anneal may be performed in an ammonia containing atmosphere. This may reduce the likelihood that any exposed AlGaN or GaN surfaces will decompose. Furthermore, as illustrated in FIG. **7**D, in some embodiments of the present invention, an encapsulation layer **520** may be deposited on a surface of the device prior to the anneal to further reduce the likelihood that exposed surfaces will decompose. It will be understood that either the ammonia, the encapsulation layer **520** or both can be used without departing from the scope of the present invention.

[0086] After the implant anneal, or as a separate anneal, a lower temperature activation anneal may be performed in an atmosphere designed to remove hydrogen form the implanted gate region **510**. This activation anneal may be similar to activation anneals performed for Mg-doped GaN. As-grown MOCVD Mg-doped GaN is not p-type. However, when annealed at a temperature of from about 600 to about 900° C. for from about 1.0 minute to about 1.0 hour in a pure N_2 or N_2/O_2 atmosphere, the as-grown GaN can be rendered p-type by removing the hydrogen from the GaN.

[0087] Source and drain contacts **30** and **31** (FIGS. **9**A and **9**B) may be formed before or after the implant anneal and the activation anneal in accordance with some embodiments of the present invention. In particular, if the implant anneal and/or activation anneal temperatures exceed a maximum threshold of the ohmic contact metals, the typical fabrication sequence has to be modified. Ohmic contact metal is typically formed before the gate process is performed, as discussed above. On the other hand, if the ohmic contact process includes an ion implantation and implant anneal, then the gate implant anneal and the ohmic implant anneal may be performed at the same time, followed by the ohmic contact metal deposition. Source and drain contacts **30** and **31** (FIGS. **9**A and **9**B) may be formed using a similar process as discussed above with respect to FIGS. **5**A and **5**B and, therefore, details of the formation thereof will not be discussed further herein.

[0088] Referring now to FIG. **7**E, the gate electrode **32** may be formed after forming the implanted gate region **510** and the annealing processes discussed above. The gate electrode **32** may not be annealed. As illustrated in FIG. **7**E, the gate electrode **32** is formed in the trench **76** on the implanted gate region **510** and the spacer layer **23**. The gate electrode **32** may have a gate length of from about 0.5 μm to about 5.0 μm. The gate electrode **32** may be a "T" gate as illustrated in FIG. **7**E and may be fabricated using conventional fabrication techniques. Suitable gate materials may include conventional materials capable of making a Schottky contact to a nitride based semiconductor material, such as Ni, Pt, $NiSi_x$, Cu, Pd, Cr, W and/or WSiN.

[0089] Furthermore, that gate metal area, defined by a liftoff technique, may include the gate implant region **510**, but may also extend onto a surface of the spacer layer **23** on both sides of the implant region **510**. The gate metal in contact with the surface of the barrier layer **22**, defined by the etched opening in the spacer layer **23**, may thus be self-aligned to the gate implant region **510**.

[0090] Referring now to FIG. **10**, a graph illustrating measurements of drain current on devices with Mg-implanted gates will be discussed. In particular, in some embodiments of